هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	Introduction to VLSI Design
Course Code:	CENX 415
Program:	B.S. in Computer Engineering
Department:	Department of Computer Engineering
College:	College of Computer and Information Sciences
Institution:	King Saud University
Version:	*Course Specification Version Number*
Last Revision Date:	*Pick Revision Date.*

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (3 hours)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (Level 9)					
4. Course general Description:					
Large-scale MOS design: MOS transistors, static and dynamic MOS gates, stick diagrams, MOS circuit fabrication, design rules, power and delay estimates, scaling, MOS combinational and sequential logic design, register and clocking schemes, memory, data-path, and control unit design. Elements of computer-aided circuit analysis and layout techniques.					
5. Pre-requirements for this course (if any)**:**					
CENX 212, Digital Logic Design 2 **EE 310, Basic Electronics**					
6. Co-requirements for this course (if any)**:**					
7. Course Main Objective(s):					
This course provides students with basic knowledge in VLSI design techniques and methodologies.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	4 hours per week	100%
2	E-learning		
3	Hybrid • Traditional classroom • E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	
3.	**Field**	
4.	**Tutorial**	15
5.	**Others (specify)**	
Total		60

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Describe how to build logic gates and data path components (memories, adders, multipliers…etc) in CMOS using multiple circuit styles.	**1**	**Lectures and Tutorials**	**Exams and Homework**
1.2	Explain how VLSI chips are designed, tested and manufactured in lights of the effects of scaling and packaging on circuits.	**1**	**Lectures and Tutorials**	**Exams and Homework**
2.0	**Skills**			
2.1	Optimize circuits using delay models and logical effort.	**2**	**Lectures and Tutorials**	**Exams and Homework**
2.2	Apply the concepts of timing; clocking, timing constraints, clock skew, jitter, and propagation delays.	**2**	**Lectures and Tutorials**	**Exams and Homework**
2.3	Describe and analyze power consumption components in VLSI circuits.	**2**	**Lectures and Tutorials**	**Exams and Homework**
3.0	**Values, autonomy, and responsibility**			

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
3.1	Design a complex system using CAD-Tools for circuit analysis and layout.	6	Lectures and Tutorials	Exams and Project

C. Course Content

No	List of Topics	Contact Hours
1.	MOS Transistors, Gates and MOS Fabrication	12
2.	Delay and Logical Effort	12
3.	Circuit Families and Combinational Circuit Design	8
4.	Data path Functional Unit Design (Adders, Multipliers… etc)	6
5.	Sequential Circuit Design	6
6.	MOS Memory, MOS Decoders	4
7.	Power Consumption	4
8.	Testing and Chip Level Issues	4
9.	Scaling, Packaging and I/O	4
Total		60

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Midterm Examination (1)	6	15%
2.	Midterm Examination (2)	12	15%
3.	Homework Assignments	Weekly	10%
4.	Project	14	20%
5.	Final Exam	End	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	Principles of CMOS VLSI Design, L. Weste Harris, 4th Edition.
Supportive References	
Electronic Materials	https://lms.ksu.edu.sa
Other Learning Materials	

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Lecture room with number of seats enough to accommodate enrolled students.
Technology equipment (projector, smart board, software)	Overhead projector with required software to facilitate presentations on smart board.
Other equipment (depending on the nature of the specialty)	

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	Department Council	Course reports are evaluated by the Department Council.
Effectiveness of Students assessment	Faculty-Peer Review	Final examination is moderated.
Quality of learning resources	Students	Indirect – Edu-gate survey.
The extent to which CLOs have been achieved	Students	Attainment level of every CLO is measured directly.
Other		

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	