هيئة تقويم التعليم والتدريب
Education & Training Evaluation Commission

2023
TP-153

Course Specification
(Bachelor)

Course Title:	Digital Logic Design II
Course Code:	CENX 212
Program:	B.S. in Computer Engineering
Department:	Department of Computer Engineering
College:	College of Computer and Information Sciences
Institution:	King Saud University
Version:	*Course Specification Version Number*
Last Revision Date:	*Pick Revision Date.*

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (4 (3,1,2) hours)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (Level 5)					
4. Course general Description:					
Topics include: registers and counters, state machines, design of datapath and control circuits, hardware description languages (HDL) and the synthesis of logic circuits on programmable logic devices such as FPGA and CPLD					
5. Pre-requirements for this course (if any)**:**					
Digital Logic Design I, CENX 211					
6. Co-requirements for this course (if any)**:**					
7. Course Main Objective(s):					
This course provides students with advanced knowledge on synchronous sequential machines and basic knowledge in programmable logic devices including hardware description language. The course includes a lab component to help students get hands-on experience with the theoretical concepts they take in the course.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	6 hours per week	100%
2	E-learning		
3	Hybrid • Traditional classroom • E-learning		
4	Distance learning		

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	30
3.	**Field**	
4.	**Tutorial**	15
5.	**Others (specify)**	
Total		90

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
1.1	Explain basic memory systems and programmable logic architectures such as ROM, SRAM, DRAM, PAL, PLA, FPGA, and CPLD.	**1**	**Lectures and Tutorials**	**Exam and Homework**
1.2	Describe the logic synthesis process that transforms an HDL description into a physical implementation.	**1**	**Lectures, Tutorials, Lab demonstration**	**Exams and Homework**
2.0	**Skills**			
2.1	Design datapath and state machine components and model them using HDL constructs.	**2**	**Lectures, Tutorials, Lab demonstration**	**Exams and Homework**
2.2	Apply the concepts of basic timing issues, including clocking, timing constraints, and propagation delays during the design process.	**2**	**Lectures, Tutorials, Lab demonstration**	**Exams and Homework**
3.0	**Values, autonomy, and responsibility**			

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
3.1	Implement a digital system in an FPGA or CPLD and evaluate the implementation characteristics such as programmable logic resources that are used and maximum clock frequency.	6	Lectures, Tutorials, Lab demonstration	Exams and Homework

C. Course Content

No	List of Topics	Contact Hours
1.	Registers, counters, and memory.	8
2.	Finite state machine design.	8
3.	Control and Datapath circuit design.	8
4.	Propagation delays and timing constraints.	4
5.	Programmable devices.	8
6.	Introductory concepts in HDL.	8
7.	Modeling and synthesis of Combinational and Sequential logic in HDL.	12
8.	Subprograms and test benches in HDL.	4
	Total	60

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Midterm Examination (1)	6	15%
2.	Midterm Examination (2)	12	15%
3.	Homework Assignments	Weekly	10%
4.	LAB	Bi-weekly	20%
5.	Final Exam (Laboratory + Theory)	End	40% (5+35)%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	• Verilog HDL (2nd Edition), Samir Palnitkar, Prentice Hall.

	• Logic and Computer Design Fundamentals (4th Edition), M. Morris Mano and Charles R. Kime, Prentice Hall.
Supportive References	• Digital Design (3rd Edition), Morris Mano, Prentice Hall. • Verilog by Example: A Concise Introduction for FPGA Design, Blaine Readler, Full Arc Press.
Electronic Materials	https://lms.ksu.edu.sa
Other Learning Materials	

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	Lecture room with number of seats enough to accommodate enrolled students.
Technology equipment (projector, smart board, software)	Overhead projector with required software to facilitate presentations on smart board.
Other equipment (depending on the nature of the specialty)	

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	Department Council	Course reports are evaluated by the Department Council.
Effectiveness of Students assessment	Faculty-Peer Review	Final examination is moderated.
Quality of learning resources	Students	Indirect – Edu-gate survey.
The extent to which CLOs have been achieved	Students	Attainment level of every CLO is measured directly.
Other		

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	